CBCS SCHEME

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BEC302

Third Semester B.E./B.Tech. Degree Examination, Dec.2023/Jan.2024
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Develop a truth table of logic which takes two , 2 – bit binary numbers as its input and generate on output equal to 1, when the sum of the two numbers is odd.	7	L1	CO1
	b.	Convert the following Boolean function into : i) $f(abc) = (\bar{a} + b)(b + \bar{c})$ – Min term canonical form. ii) $f(xyz) = x + \bar{x}\,\bar{z}(y + \bar{z})$ – Max term canonical form.	7	L1	CO1
	c.	List the difference between Prime implicant and Essential prime implicant.	6	L1	CO1
		OR			
Q.2	a.	Simplify the given Boolean function using Quine Mc Cluskey Minimization Technique for the function $R = f(abcd) = \Sigma(0, 1, 2, 6, 7, 9, 10, 12) + dc(3, 5)$.	10	L1	CO1
	b.	Find the minimal sum and minimal product for the given function using K – map method for the function $R = f(abcd) = \Sigma m(0, 1, 3, 7, 8, 12) + dc(5, 10, 13, 14)$.	10	L1	CO1
		Module – 2			
Q.3	a.	List the difference between decoder and encoder and implement full adder using IC – 74138.	10	L3	CO2
	b.	What is Comparator? Design a 2 – bit digital comparator.	10	L3	CO2
		OR			
Q.4	a.	Realize the Boolean function $P = f(wxyz) = \Sigma(0, 1, 5, 6, 7, 10, 15)$ using i) 8 : 1 MUX ii) 4 : 1 MUX.	10	L2	CO2
	b.	With neat logic diagram, explain carry ahead adder.	10	L2	CO2
		Module – 3			
Q.5	a.	Explain the working of master slave JK flip flop with help of Logic diagram , Function table , Logic symbol and Timing diagram.	10	L1	CO3
	b.	Obtain the characteristic equation for : i) SR flip - flop ii) J – K – flip - flop iii) D – flip - flop iv) T – flip - flop.	10	L2	CO3
		OR			

<table>
<tr><td>Q.6</td><td>a.</td><td>Design a Synchronous 3 – bit up counter using J K – flip - flop.</td><td>10</td><td>L4</td><td>CO3</td></tr>
<tr><td></td><td>b.</td><td>Design a 4 – bit universal shift register using positive edge triggered D – flip - flop and 4 : 1 MUX , to operate as shown in table below :
<table>
<tr><th>S_1</th><th>S_0</th><th>Register Operation</th></tr>
<tr><td>0</td><td>0</td><td>- Hold</td></tr>
<tr><td>0</td><td>1</td><td>- Shift right</td></tr>
<tr><td>1</td><td>0</td><td>- Shift left</td></tr>
<tr><td>1</td><td>1</td><td>- Parallel load operation</td></tr>
</table></td><td>10</td><td>L4</td><td>CO3</td></tr>
<tr><td colspan="6">Module – 4</td></tr>
<tr><td>Q.7</td><td>a.</td><td>Illustrate the structure and verilog module and write a verilog code for Half – adder using structural model.</td><td>10</td><td>L3</td><td>CO4</td></tr>
<tr><td></td><td>b.</td><td>What are different types of operators used in HDL with example?</td><td>10</td><td>L2</td><td>CO4</td></tr>
<tr><td colspan="6">OR</td></tr>
<tr><td>Q.8</td><td>a.</td><td>Illustrate the structure of Data flow description with example.</td><td>10</td><td>L3</td><td>CO4</td></tr>
<tr><td></td><td>b.</td><td>Write the syntax of conditional signal assignment statement. Write a code for 4 : 1 MUX using conditional signal statement.</td><td>10</td><td>L2</td><td>CO4</td></tr>
<tr><td colspan="6">Module – 5</td></tr>
<tr><td>Q.9</td><td>a.</td><td>Write the structure of Verilog behavioral description.</td><td>6</td><td>L2</td><td>CO4</td></tr>
<tr><td></td><td>b.</td><td>Write the syntax of IF statement with example.</td><td>7</td><td>L2</td><td>CO4</td></tr>
<tr><td></td><td>c.</td><td>Write a code for D – Latch using Behavioral description.</td><td>7</td><td>L2</td><td>CO4</td></tr>
<tr><td colspan="6">OR</td></tr>
<tr><td>Q.10</td><td>a.</td><td>Write the syntax of While loop statement with example.</td><td>10</td><td>L2</td><td>CO4</td></tr>
<tr><td></td><td>b.</td><td>Write a verilog code of a 3 – bit ripple carry adder using Structural description method.</td><td>10</td><td>L2</td><td>CO4</td></tr>
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